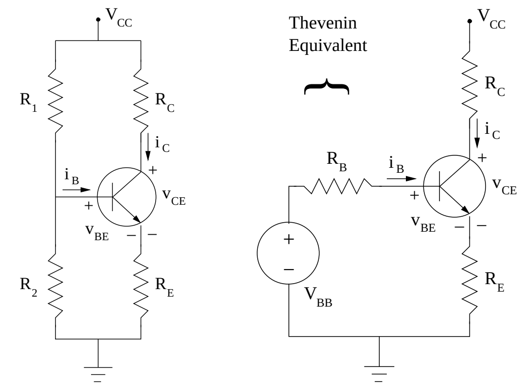
Alternative Biasing Schemes

We discussed using an emitter resistor to stabilize the bias point (Q point) of a BJT amplifier as is shown (R_c can be zero). There are two issues associated with this bias configuration (called :bias with one power supply") which may make it unsuitable for some applications.

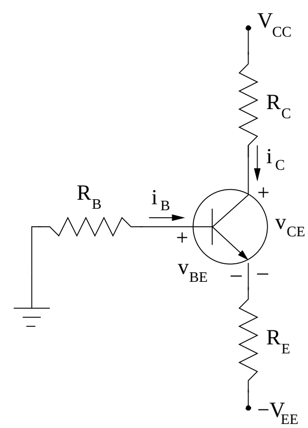


1) Because $V_B > 0$, a coupling capacitor is typically needed to attach the input signal to the amplifier circuit.

The combination of the coupling capacitor and the input resistance of the amplifier leads to a lower cut-off frequency for the amplifier as we discussed before, *i.e.,* this biasing scheme leads to an "AC" amplifier. In some applications, we need "DC" amplifiers. Biasing with two voltage sources, discussed below, will solve this problem.

2) Biasing with one voltage source requires 3 resistors (R_1, R_2, and R_E), a coupling capacitor, and possibly a by-pass capacitor. In integrated circuit chips, resistors and large capacitors take too much space. It is preferable to reduce their number as much as possible and replace their function with additional transistors. For IC applications, "current-mirrors" are usually used to bias the circuit as is discussed below.

Biasing with 2 Voltage Sources:



Consider the biasing scheme as is shown. This biasing scheme is similar to bias with one voltage source. Basically, we have assigned a voltage of $-V_{EE}$ to the ground (reference voltage) and chosen $V_{EE} = V_{BB}$. As such, all of the currents and voltages in the circuit should be identical to the bias with one power supply. We should find that this is a stable bias point as long as $R_B \ll \beta R_E$. This is shown below:

KVL-BE: $R_B I_B + V_{BE} + R_E I_E - V_{EE} = 0$

$$I_E \approx I_C = \beta I_B$$

$$R_B \frac{I_E}{\beta} + R_E I_E = V_{EE} - V_{BE} \quad \rightarrow \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Similar to the bias with one power supply, if we choose R_B such that, $R_B \ll \beta R_E$, we get:

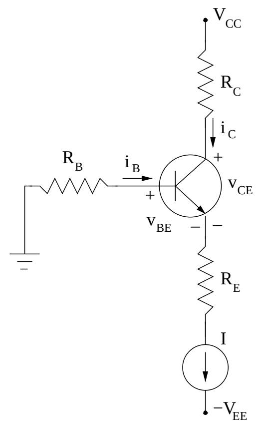
$$I_C \approx I_E \approx \frac{V_{EE} - V_{BE}}{R_E} = const$$

KVL-CE: $V_{CC} = R_C I_C + V_{CE} + R_E I_E - V_{EE}$

$$V_{CE} = V_{CC} + V_{EE} + I_C(R_C + R_E) = const$$

Therefore, I_E, I_C, and V_{CE} will be independent of BJT parameters (*i.e.,* BJT β) and we have a stable bias point. Similar to stable bias with one power supply, we also need to ensure that $R_E I_E \geq 1$ V to account for small possible variation in V_{BE}.

Bias with two power supplies has certain advantages over biasing with one power supply, it has two resistors, R_B and R_E (as opposed to three), and in fact, in most applications, we can remove R_B altogether. In addition, in some configuration, we can directly couple the input signal to the amplifier without using a coupling capacitor (because $V_B \approx 0$). As such, such a configuration can also amplify "DC" signals.



Both stable biasing schemes, with one or two power supplies, use R_E as a negative feedback to "fix" I_E and make it independent of BJT parameters. In effect, any biasing scheme which results in a constant I_E, independent of BJT parameters, will be a stable biasing technique.

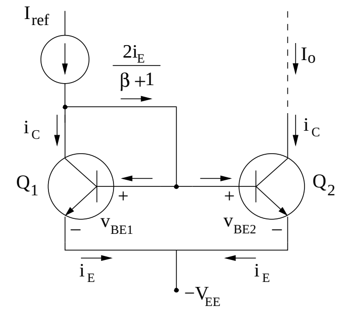
Schematically, all these biasing schemes can be illustrated with an ideal current source in the emitter circuit as is shown. For the circuits which include a current source, resistor R_E is NOT needed for stable biasing anymore. For example, for a common emitter amplifier, it can be removed from the circuit. For a CE amplifier with emitter resistance, value of R_E is set by "AC" gain requirements and not by bias stability.

Because of elimination of R_B and R_E (or reducing R_E), biasing with a current source is the preferred way in most integrated circuits. Such a biasing can be achieved with a current mirror circuit.

Current Mirrors

A large family of BJT circuit, including current mirrors, differential amplifiers, and emitter-coupled logic circuits include identical BJT pairs. In most cases, two identical BJTs are manufactured together on one chip in order to ensure that their parameters are approximately equal (Note that if you take two commercial BJTs, *e.g.,* two 2N3904, there is no guaranty that $\beta_1 = \beta_2$, while if they are grown together on a chip, $\beta_1 \approx \beta_2$. For our analysis, we assume that both BJTs are identical.)

Consider the circuit shown with identical transistors, Q_1 and Q_2. Because both bases and emitters of the transistors are connected together, KVL leads to $v_{BE1} = v_{BE2}$. As we discussed before, BJT operation is controlled by v_{BE}. As $v_{BE1} = v_{BE2}$ and transistors are identical, they should have similar i_E, i_B and i_c:



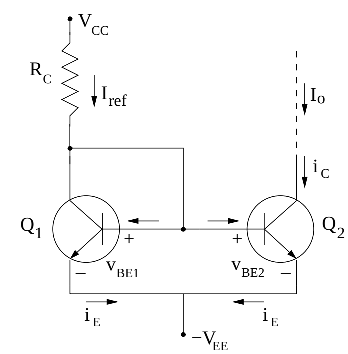
$$i_B = \frac{i_E}{\beta + 1} \qquad I_o = i_c = \frac{\beta i_E}{\beta + 1}$$

KCL: $$I_{ref} = i_c + \frac{2i_E}{\beta + 1} = \frac{i_E}{\beta + 1} + \frac{2i_E}{\beta + 1} = \frac{\beta + 2}{\beta + 1}\, i_E$$

$$\frac{I_o}{I_{ref}} = \frac{\beta}{\beta + 2} = \frac{1}{1 + 2/\beta}$$

(We have used $i_C = \beta i_B$ and $i_E = (\beta + 1) i_B$ to illustrate impact of β.) For $\beta \gg 1$, $I_o \approx I_{ref}$ (with an accurancy of $2/\beta$). This circuit is called a "current mirror" as the two transistors work in tandem to ensure that current I_o remains the same as I_{ref} no matter what circuit is attached to the collector of Q_2. As such, the circuit behaves as a current source and can be used to bias BJT circuits.

Value of I_{ref} can be set in many ways. The simplest is by using a resistor R_c as is shown. By KVL, we have:

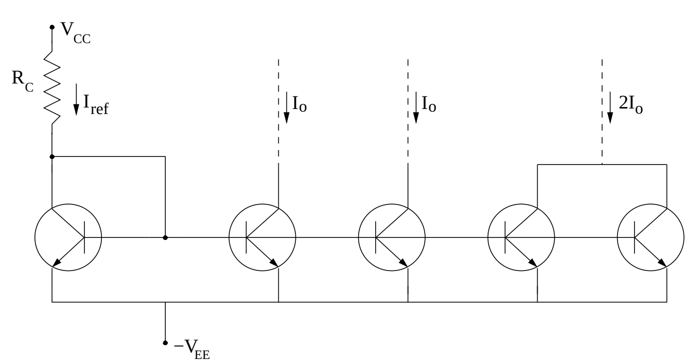


$$V_{CC} = R_C I_{ref} + v_{BE1} - V_{EE}$$

$$I_{ref} = \frac{V_{CC} + V_{EE} - v_{BE1}}{R_C} = const$$

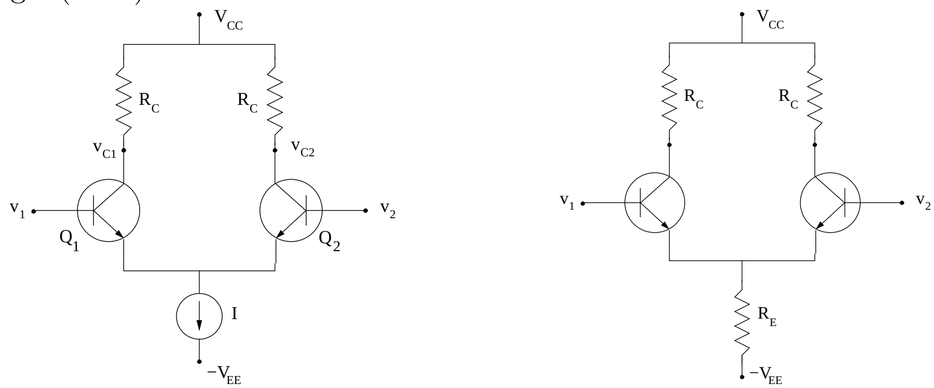
Current mirror circuits are widely used for biasing BJTs. In the simple current mirror circuit above, $I_o = I_{ref}$ with a relative accuracy of $2/\beta$ and I_{ref} is constant with an accuracy of small changes in v_{BE1}. Variation of current mirror circuit, such as Wilson current mirror and Widlar current mirror (See Sedra and Smith) are available that lead to $I_o = I_{ref}$ with a higher accuracy and compensate for $2/\beta$ and changes in v_{BE} effects. Wilson mirror is especially popular because it replace R_c with a transistor.

The right hand part of the current mirror circuit can be duplicated such that one current mirror circuit can bias several BJT circuits as is shown. In fact, by coupling output of two of the right hand parts, integer multiples of I_{ref} can be made for biasing circuits which require a higher bias current.



BJT Differential Pairs: Emitter-Coupled Logic and Difference Amplifiers

The differential pairs are the most widely used circuit building block in analog ICs. They are made from both BJT and variant of Field-effect transistors (FET). In addition, BJT differential pairs are the basis for the very-high-speed logic circuit family called Emitter-Coupled Logic (ECL).



The circuit above (on the left) shows the basic BJT differential-pair configuration. It consists of two matched BJTs with emitters coupled together. On ICs, the differential pairs are typically biased by a current source as is shown (using a variant of current mirror circuit). The differential pair can be also biased by using an emitter resistor as is shown on the circuit above right. This variant is typically used when simple circuits are built from individual components (it is not very often utilized in modern circuits). Here we focus on the differential pairs that are biased with a current source.

The circuit has two inputs, v_1 and v_2 and the output signals can be extracted from the collector of both BJTs (v_{C1} and v_{C2}). Inspection of the circuit reveal certain properties. By KCL we find that $i_{C1} + i_{C2} \approx i_{E1} + i_{E2} = I$. That is the two BJTs share the current I between them. So, in general, $i_{C1} \approx i_{E1} \leq I$ and $i_{C2} \approx i_{E2} \leq I$. It is clear that at least one of the BJT pair should be ON (*i.e.*, not in cut-off) in order to satisfy the above equation (both i_{E1} and i_{E2} cannot be zero). Value of R_C is chosen such that either BJT will be in active-linear if its collector current reaches its maximum value of I.

$$V_{CC} = R_C i_{C1} + v_{CE1} + V_{ICS} - V_{EE}$$

$$v_{CE1} = V_{CC} + V_{EE} + V_{ICS} - R_C i_{C1} > v_\gamma$$

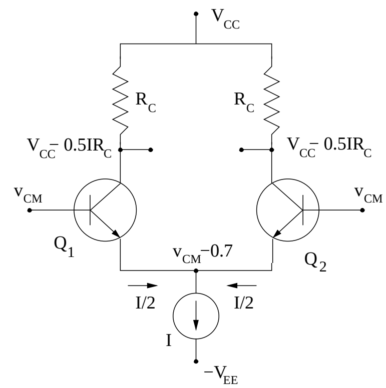
$$R_C < \frac{V_{CC} + V_{EE} + V_{ICS}}{I} < \frac{V_{CC} + V_{EE}}{I}$$

With this choice for R_C, both BJTs will either be in cut-off or active-linear (and never in saturation).

Lastly, if we write a KVL through a loop that contains the input voltage sources and both base-emitter junctions, we will have:

$$\text{KVL:} \quad -v_1 + v_{BE1} - v_{BE2} + v_2 = 0 \quad \rightarrow \quad v_{BE1} - v_{BE2} = v_1 - v_2$$

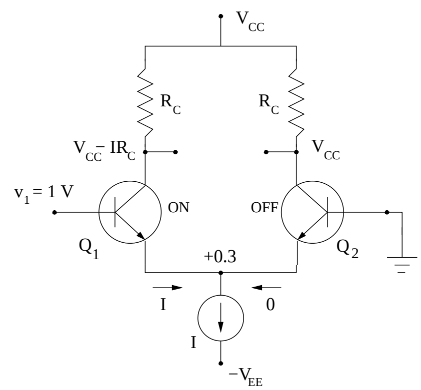
To understand the behavior of the circuit, let's assume that a common voltage of v_{CM} is applied to both inputs: $v_1 = v_2 = v_{CM}$ (CM stands for Common Mode). Then, $v_{BE1} - v_{BE2} = v_1 - v_2 = 0$ or $v_{BE1} = v_{BE2}$. Because identical BJTs are biased with same v_{BE}, we should have $i_{E1} = i_{E2}$ and current I is divided equally between the pair:



$$\text{KCL:} \quad i_{C1} \approx i_{E1} = 0.5I \quad \text{and} \quad i_{C2} \approx i_{E2} = 0.5I.$$

As such, both BJTs will be in active linear, $v_{BE1} = v_{BE2} = 0.7$ V and the output voltages of $v_{C1} = v_{C2} = v_{CC} - 0.5IR_C$ will appear at both collectors.

Now, let's assume $v_1 = 1$ V and $v_2 = 0$. Writing KVL on a loop that contains both input voltage sources, we get:



$$\text{KVL:} \quad v_{BE1} - v_{BE2} = v_1 - v_2 = 1 \text{ V}$$

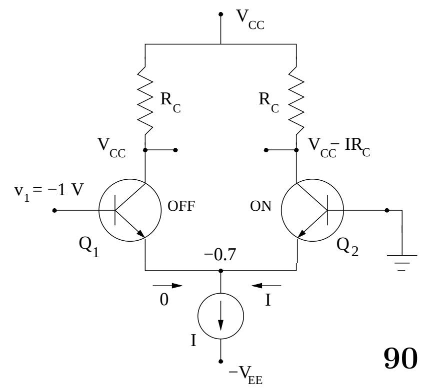
Because $v_{BE} \leq v_\gamma = 0.7$ V, the only way that the above equation can be satisfied is for v_{BE2} to be negative: Q_2 is in cut-off and $i_{E2} = 0$. Because of the current sharing properties, Q_1 should be on and carry current I. Thus:

$$v_{BE1} = 0.7 \text{ V}, \quad v_{BE2} = v_{BE1} - 1 = -0.3 \text{ V}$$

$$i_{C1} = i_{E1} = I, \quad i_{C2} = i_{E2} = 0$$

And voltages of $v_{C1} = V_{CC} - IR_C$ and $v_{C2} = V_{CC}$ will develop at the collectors of the BJT pair. One can easily show that for any $v_1 - v_2 > v_\gamma = 0.7$ V, Q_1 will be ON with $i_{C1} = i_{E1} = I$ and $v_{C1} = V_{CC} - IR_C$; and Q_2 will be OFF with $i_{C2} = i_{E2} = 0$ and $v_{C2} = V_{CC}$.

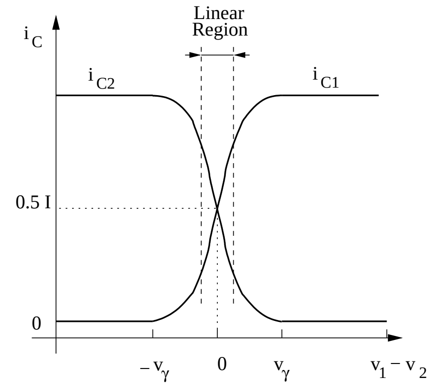
If we now apply $v_1 = -1$ V and $v_2 = 0$, the reverse of the above occurs:



$$\text{KVL:} \quad v_{BE1} - v_{BE2} = v_1 - v_2 = -1 \text{ V}$$

In this case, Q_2 will be ON and carry current I and Q_1 will be OFF. Again, it is easy to show that this is true for any $v_1 - v_2 < -v_\gamma = -0.7$ V.

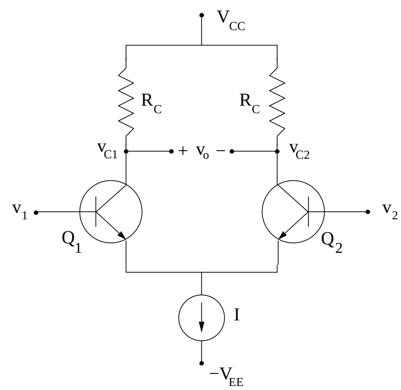
The response of the BJT differential pair to a pair of input signals with $v_d = v_1 - v_2$ is summarized in this graph. When v_d is large, the collector voltages switch from one state v_{CC} to another state $v_{CC} - IR_C$ depending on the sign v_d. As such, the differential pair can be used as a logic gate and a family of logic circuits, emitter-coupled logic, is based on differential pairs. In fact, because a BJT can switch very rapidly between cut-off and active-linear regimes, ECL circuits are the basis for the fastest logic circuits available today.



For small v_d (typically ≤ 0.2 V), the circuit behaves as a linear amplifier. In this case, the circuit is called a differential amplifier and is the most popular building block of analog ICs.

Differential Amplifiers

The properties of the differential amplifier above (case of v_d small) can be found in a straight-forward manner. The input signals v_1 and v_2 can be written in terms of their difference $v_d = v_1 - v_2$ and their average (common-mode voltage v_{CM}) as:



$$v_{CM} = \frac{v_1 + v_2}{2} \quad \text{and} \quad v_d = v_1 - v_2$$
$$v_1 = v_{CM} + 0.5 v_d$$
$$v_2 = v_{CM} - 0.5 v_d$$

The response of the circuit can now be found using superposition principle by considering the response to: case 1) $v_1 = v_{CM}$ and $v_2 = v_{CM}$ and case 2) $v_1 = 0.5 v_d$ and $v_2 = -0.5 v_d$. The response of the circuit to case 1, $v_1 = v_2 = v_{CM}$, was found in page 92. Effectively, v_{CM} sets the bias point for both BJTs with $i_{C1} = i_{E1} = i_{C2} = i_{E2} = 0.5I$, collector voltages of $v_{C1} = v_{C2} = v_{CC} - 0.5IR_C$, and a difference of zero between to collector voltages, $v_o = v_{C1} - v_{C2} = 0$.

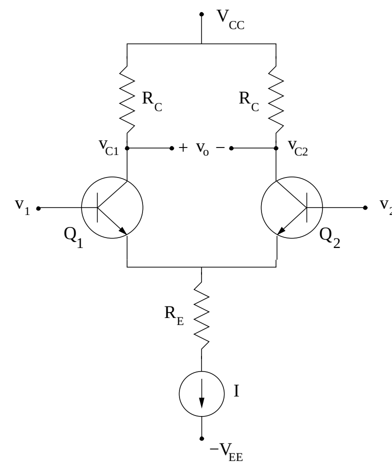
To find the response of the circuit to case 2, $v_1 = 0.5 v_d$ and $v_2 = -0.5 v_d$, we can use our small signal model (since v_d is small). Examination of the circuit reveals that each of the BJTs form a common emitter amplifier configuration (with no emitter resistor). Using our analysis of common emitter amplifiers ($A_v = R_C / r_e$), we have:

$$v_{c1} = A_v v_i = \frac{R_C}{r_e}(0.5 v_d) \quad \text{and} \quad v_{c2} = A_v v_i = \frac{R_C}{r_e}(-0.5 v_d)$$
$$v_o = v_{c1} - v_{c2} = \frac{R_C}{r_e} v_d$$

Summing the responses for case 1 and 2, we find that the output voltage of this amplifier is

$$v_o = 0 + \frac{R_C}{r_e} v_d = \frac{R_C}{r_e} v_d \quad \rightarrow \quad A_v = \frac{R_C}{r_e}$$

similar to a common emitter amplifier. The additional complexity of this circuit compared to our standard common emitter amplifier results in three distinct improvements:
1) This is a "DC" amplifier and does not require a coupling capacitor.
2) Absence of biasing resistors ($R_b \rightarrow \infty$) leads to a higher input resistance, $R_i = r_\pi \parallel R_B = r_\pi$.
3) Elimination of biasing resistors makes it more suitable for IC implementation.



It should be obvious that a differential amplifier configuration can be developed which is similar to a common emitter amplifier with a emitter resistor (to stabilize the gain and increase the input resistance dramatically). Such a circuit is shown. Note that R_E in this circuit is not used to provide stable DC biasing (current source does that). Its function is to provide negative feedback for amplification of small signal, v_d. Following the above procedure, one can show that the gain of this amplifier configuration is:

$$v_o = \frac{R_C}{R_E + r_e} v_d \quad \rightarrow \quad A_v = \frac{R_C}{R_E + r_e}$$

As with standard CE amplifer with emitter resistance, the input impdenace is also increased dramatically by negative feedback of R_E (and absence of biasing resistors, $R_b \rightarrow \infty$):

$$R_i = R_B \parallel [\beta(R_{E1} + r_e)] = \beta(R_{E1} + r_e)$$